CAREER EPISODE 3

INTRODUCTION

CE 3.1 During a period of 5 months starting from [redacted] I worked on a project titled Low noise and high IP3 amplifier MMIC design in the academic setting of [redacted] Under the guidance of my supervisor, [redacted], I worked on minimizing noise while maximizing the third order intercept point in the circuit. Through simulations and design, I improved my skills in high frequency circuitry and gained valuable insights into practical applications.

BACKGROUND

CE 3.2 During my studies, I worked on an extensive individual project for the Microwave Electronics course. I created a low noise high third order intercept point (IP3) amplifier Monolithic Microwave Integrated Circuit (MMIC) using CREE's Process Design Kit (PDK) based on Gallium Nitride (GaN) semiconductor technology. Using Advance Design Systems (ADS) software from Keysight, I designed and simulated this MMIC, recognizing its advantages over Printed Circuit Boards (PCBs) due to its compactness, elimination of post design soldering and improved repeatability without the uncertainties of SMD components or bond wires. GaN technology's broader band gaps, higher voltage capacity and increased electron velocity make it perfect for high power applications in communication transcriber chains, reducing RF noise in weak signals and preserving linearity in strong ones.

CE 3.3 I conducted extensive research into amplifier design methodologies, specifically the low noise and high IP3 requirements. Understanding the significance of MMICs over PCBs, I explored CREE's GaN semiconductor technology and the associated PDK. I then moved to the planning, set the objectives, using my familiarity with ADS software, I delved into its capabilities, familiarized myself with its tools and functionalities essential for MMIC design. As the project progressed, I documented each step and compiled a report detailing the design process, simulation results and performance evaluations. Upon completion, I prepared a presentation including the journey of the project, the key strategies, challenges faced and the achieved outcomes.

PROJECT REPORTING HIERARCHY

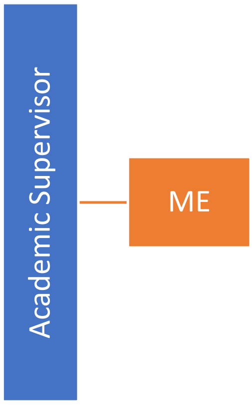


Figure 1: Hierarchy

PERSONAL ENGINEERING ACTIVITIES

CE 3.4 In design preparation, I studied the specified parameters and available resources to estimate the topology required for the project. With a 28 V drain supply and a frequency range of 5.985 GHz to 6.615 GHz, maintaining 50 Ω source and load impedance was imperative. The design also required unconditional suitably from 10 MHz to 8 MHZ, with stringent requirements for input and output reflection losses, small signal gain, noise figure, output saturation power, P2dB and IP3. Given the influence of technology on critical features like small signal gain, output power, noise figure and linearity, the chosen topology was crucial. These specifications dictated the topology; a 2-stage design with specific matching networks at the input, inter stage and output sections. I selected HEMTs with gate peripheries of 2x130 µm and 2x750 µm due to their suitability for high frequency operations and higher linearity.

CE 3.5 Considering these parameters, I used ADS software, set up the topology and ran simulations. Through iterative adjustments and detailed simulations, I adjusted the various aspects, from input and output matching networks to transistor dimensions and biasing schemes. I analyzed the circuit behavior, focused on its gain, noise figure, linearity and power handling capabilities. Each simulation run and adjustment brought me closer to the optimal design that met the specifications mentioned at the project's outset.

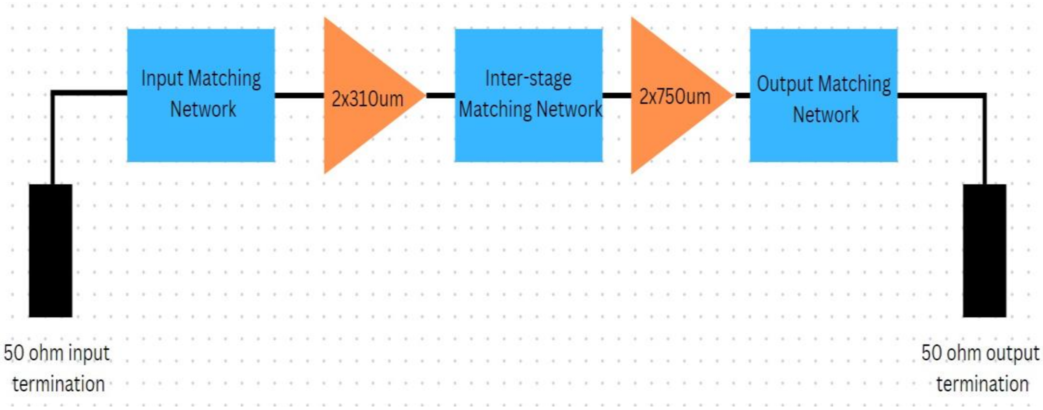
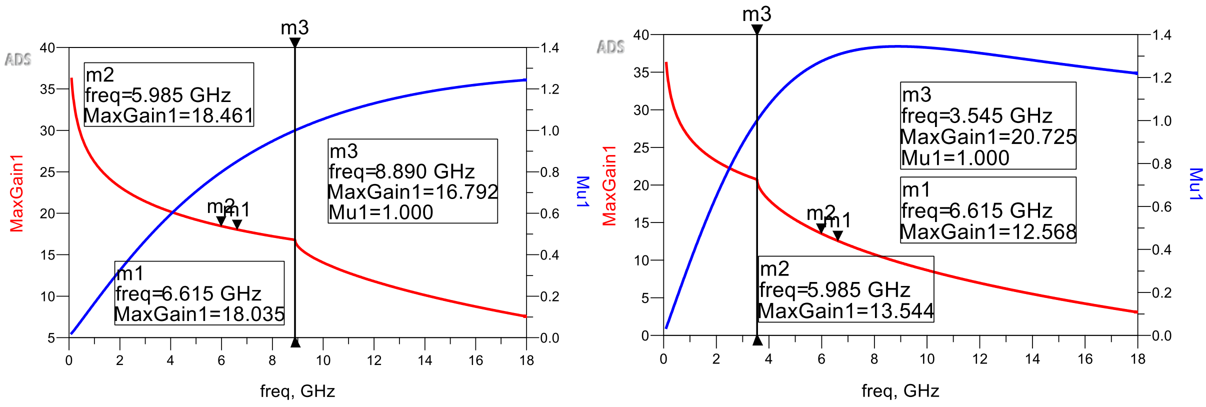


Figure 2: Amplifier design topology

CE 3.6 In my exploration of the chosen topology, I sought to ensure it met the required small gain and output power requisites. To gauge the Maximum Available Gain (MAG) for estimating achievable gain with proper impedance matching networks, I examined MAG for both stages of the design. The first stage in the frequency band of interest, showcased a minimum MAG of about 18 dB, while the second stage exhibited 12.6 dB. This 2-stage configuration resulted in a total minimum MAG of 30.6 dB. Evaluating the transistor stability, denoted by Mu was important, A Mu greater than 1 signified unconditional stability, indicating that the transistor could be terminated with any impedance without oscillation.

CE 3.7 To improve the stability, I introduced losses in frequency bands where instability was observed. For the first stage HEMT, I added a shunt resistor at drain side, avoiding losses on the gate side to mitigate noise figure impact. Conversely, for second stage HEMT, I introduced a shunt resistor at the gate to maintain output power. After implementing stability measures, both transistors exhibited Mu > 1 which indicated unconditional stability across the frequency range. However, the introduction of losses for stability resulted in a trade-off that reduced the minimum MAG in the frequency band of interest to 14.5 dB for the first stage and 12.4dB for the second, the total MAG at 26.9 dB post-stability measures, highlighting stability versus gain balance. Despite this, a sufficient margin remained for potential mismatch losses for a viable design with improved stability while accommodating practical variations.

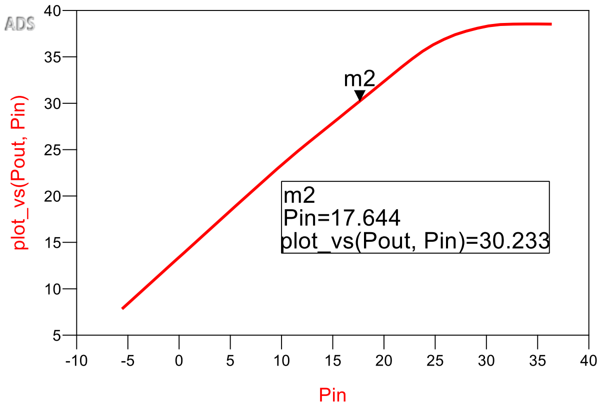


(a) 2x310um HEMT *(b) 2x750um HEMT*

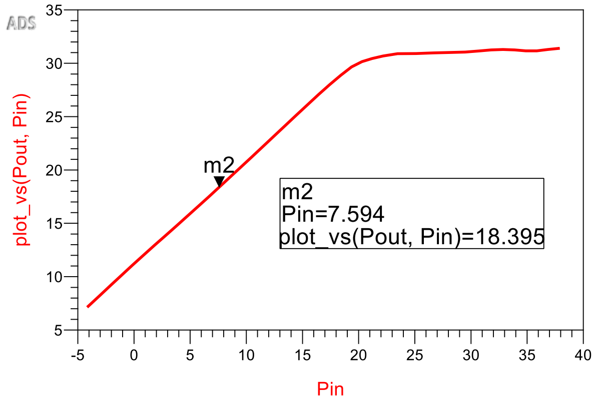
Figure 3: HEMTs MAG and Mu before stability

CE 3.8 In evaluating the topology, my considerations extended to the output power and linearity of the chosen HEMTs. The responsibility for output mainly fell on the second stage in the design. Through evaluations of CREE's GaN HEMTs, I established that these components could yield approx. 5W/ mm when optimally matched for power delivery. With a total periphery of 1.5 mm for the output stage, an expected output of 7.5 W equivalent to approx. 38.75 dBm was predicted. However, the specified requirement was a modest 1W-30dBm output power. It was important to ensure that if the saturated output power (Psat) approached this requirement closely, it would not cause gain compression in the second stage. Such compression would compromise linearity and consequently lower the desired IP3 and important specifications.

CE 3.9 I plotted graph, showcasing the delivered power versus output power of the HEMTs. This visual representation affirmed that at an output power of 30 dBm, the gain of the second stage remained uncompromised. This revelation indicated that the second stage could efficiently output 1 W of power with an input requirement of around 17.6 dBm. Factoring in the losses of the inter stage matching network estimated at 0.8 dB, I concluded that the first stage would output approx. 18.4 dBm to meet the specified output power. The linear trend of the graph also provided reassurance that the gain of first stage remained uncompromised. This analysis empowered me to assert confidently that both stages could operate efficiently without comprising linearity or output power.



(a) 2x310um HEMT



(b) 2x750um HEMT

Figure 4: Delivered power vs Output power of HEMTs

CE 3.10 After this I designed the matching networks. Understanding that the first stage held the greatest impact on noise figure, I aimed to achieve both a good noise figure and substantial gain from the first stage HEMT. To achieve a good gain, minimizing reflection losses was imperative. Consequently, the gate of the first stage needed to oppose the conjugate of the input impedance, eventually matching it to 50 Ω to meet the input reflection loss specification. Using the simulation tool, I plotted available gain and noise figure circles. These circles helped me identify the source impedance required to achieve MAG and the minimum possible noise figure (NFmin). However, the centers of the noise circle were distant which indicated a tradeoff between optimizing gain and noise figure.

CE 3.11 To mitigate this disparity and stabilize HEMT, I applied source degeneration by terminating the source with an inductor. This approach successfully brought the centers of the gain and noise circles closer. With centers now in proximity, achieving both an optimal gain and a commendable noise figure from the first stage became more feasible. Finally, I proceeded with input matching to make it as per the objectives, resulting in the creation of the input matching network. This network design integrated mandatory components like DC block and RF chokes for isolation between the RF source and DC voltage/ currents. This approach prevented exposure of RF source to DC components and vice versa for the integrity of both RF and DC signals in the circuit.

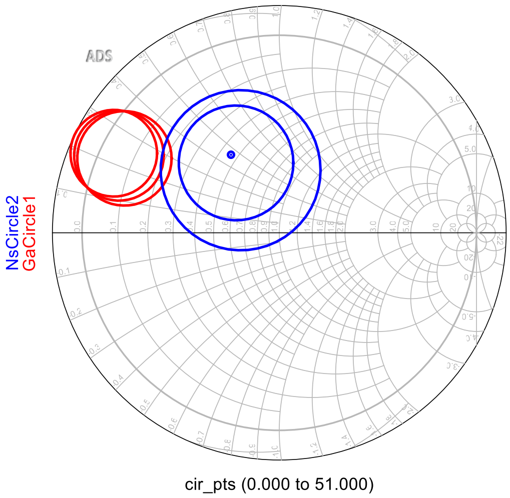


Figure 5: Gain and noise mismatch circles pre-source degeneration

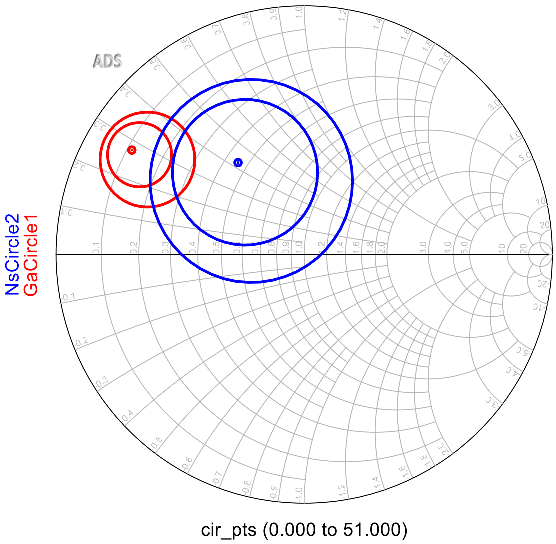


Figure 6: Gain and noise mismatch circles after degeneration

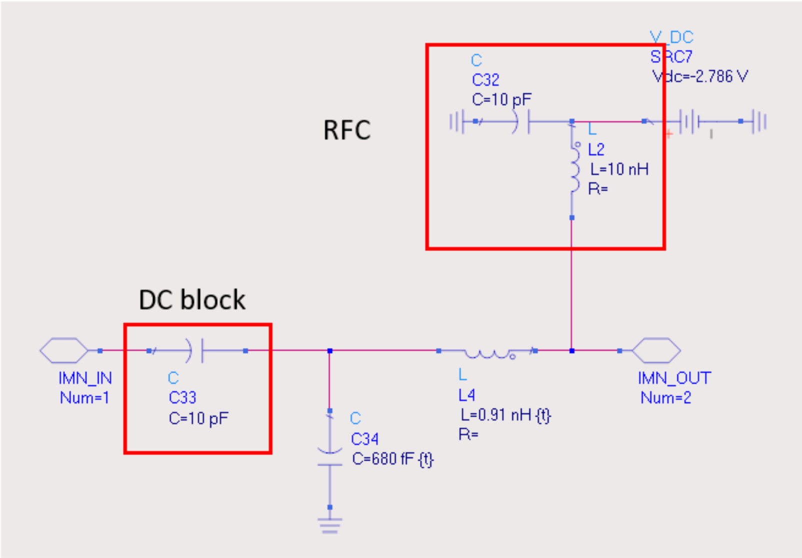


Figure 7: Input matching network using ideal components

CE 3.12 To achieve the high-power output, I designed the output matching networks which was a crucial component. The main goal was to match the optimal load impedance for power to 50 Ω for efficient power delivery. However, a significant challenge emerged due to the requirement of a maximum output reflection loss of -15 dB, balancing output power impedance of the second stage HEMT. To address this, I created the output matching network. This network aimed to strike a balance between maximizing power delivery efficiency and meeting the requirements of maintaining the output reflection loss in the specified limits. I selected the components used in this network and configured them to achieve the desired impedance transformation and minimize reflection losses thereby optimizing the power output of the second stage HEMT.

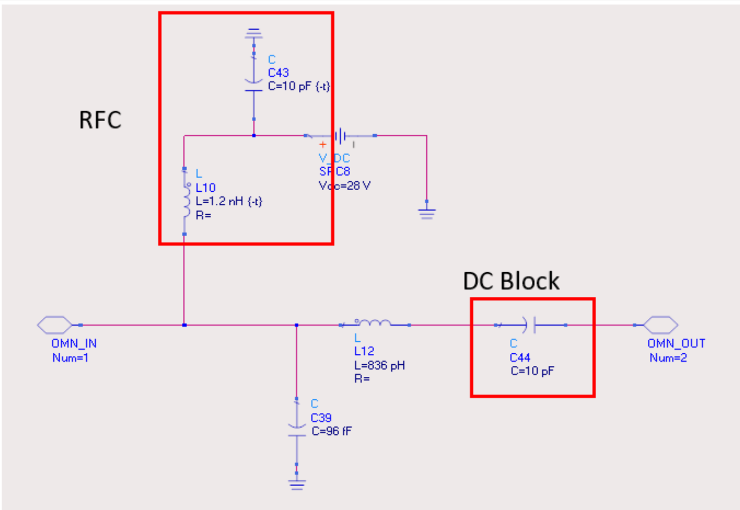


Figure 8: Output matching network using ideal components

CE 3.13 Lastly, I designed the inter-stage matching network. I designed it to match the conjugate of output impedance of the first stage to the conjugate of the input impedance of the second stage. Basically, the aim of the inter-stage matching network was to minimize the mismatch losses from stage 1 to stage 2. Moreover, it served dual-purpose apart from reducing mismatch losses, it improved the gain ripple within the amplifier. To validate the design and evaluate its compliance with the required specifications, I generated symbols representing these three matching networks. These symbols provided the easy implementation of a test bench for conducting simulations to verify the performance of design.

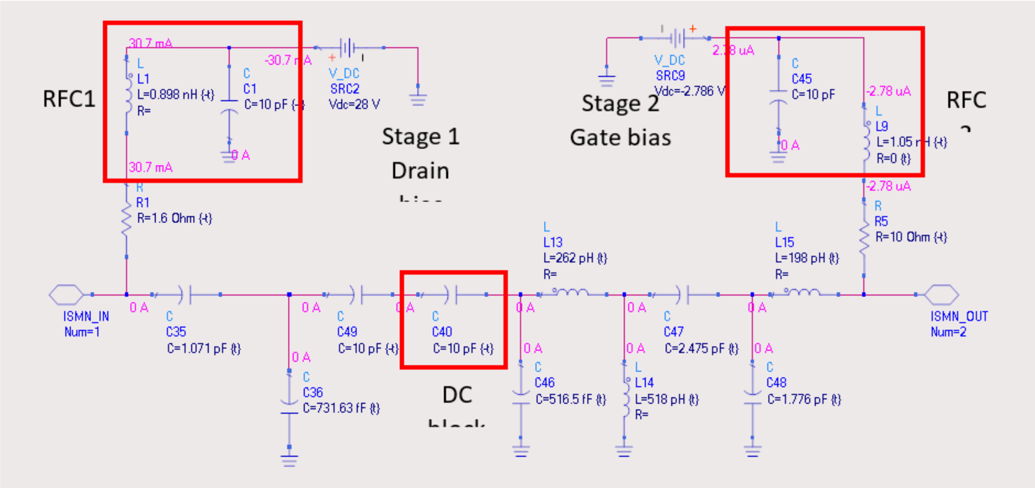


Figure 9: Inter-stage matching network using ideal components

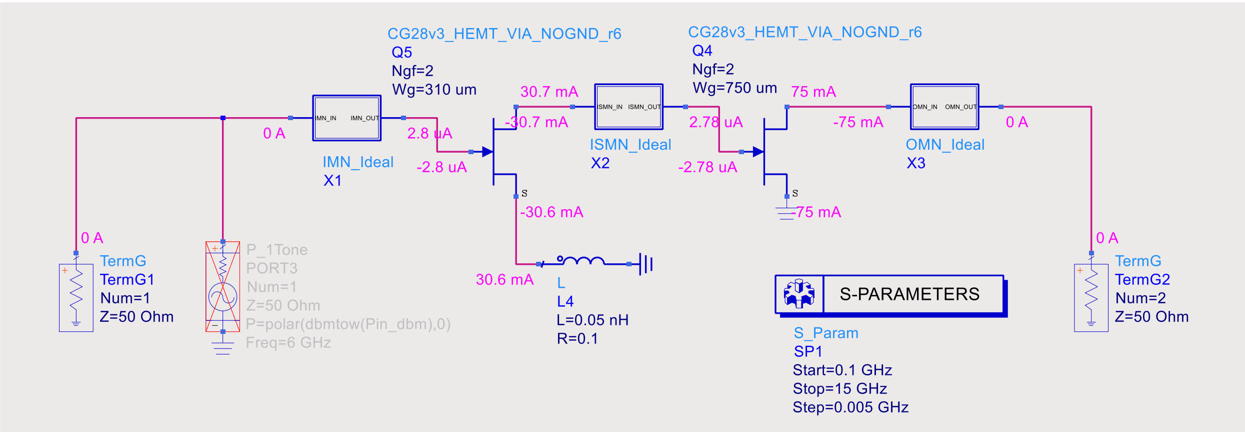
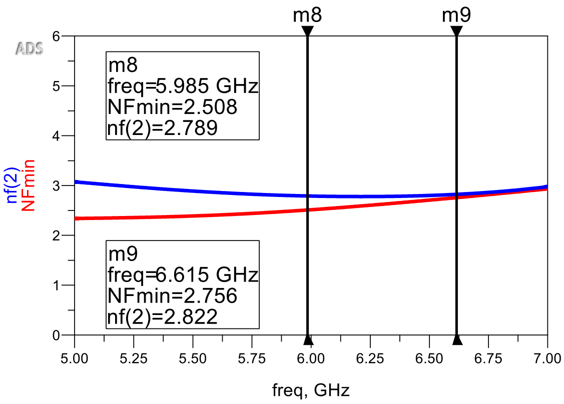
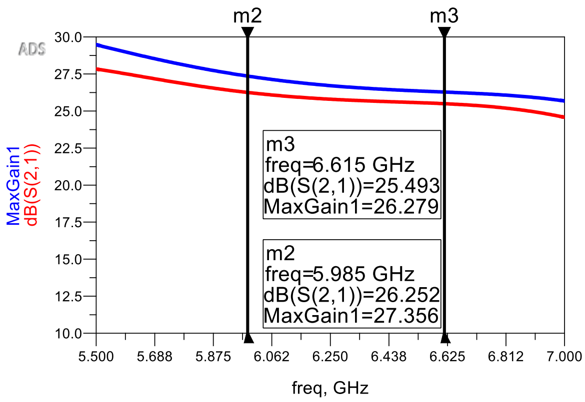


Figure 10: Schematic test bench for small signal simulations

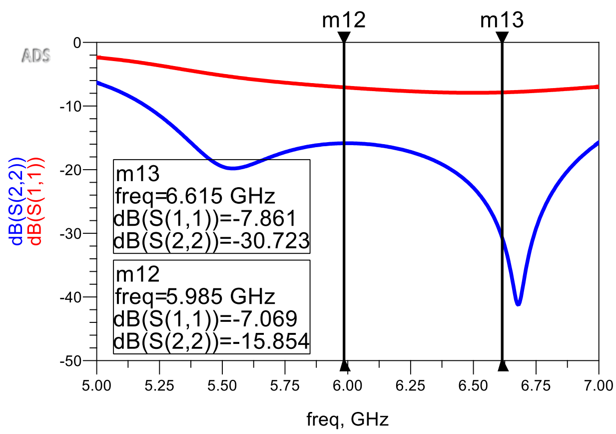
CE 3.14 Using the ideal components, I obtained small signal simulation results for the amplifier design. These simulation results proved important in evaluating various performance parameters crucial to the success of the design. The simulations confirmed the unconditional stability of the entire design, denoted by Mu consistently surpassing 2 across the frequency range. The difference between NFmin and nf(2) provided insights into the deviation between the actual source impedance and the optimum source impedance for noise. The noise figure which was a maximum of 2.789 dB was as per the requirement of 3.8 dB. The achieved gain measured approx. 25.9 dB, exhibiting a slight ripple of about ± 3.5 dB. The parameters like input and output reflection losses represented by S11 and S22 were also confirmed to be in the specified ranges. The simulation results validated the ability of the design to minimize reflection losses due to impedance mismatches at the input and output planes for optimal signal transmission through the amplifier circuit.



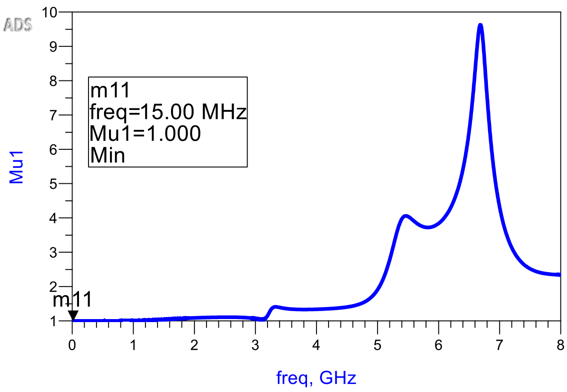
(a) Noise Figure and Nfmin



(b) Gain, S21



c) IRL and ORL



d) Mu

Figure 11: Amplifier small signal response using ideal components

CE 3.15 In analyzing the amplifier response, I delved into harmonic balance simulations to examine its large signal behavior. The results provided crucial insights into the design's performance under practical operating conditions. These simulations explained the relationship between IP3 and input power available which served as an indicator of linearity and provided a clear understanding of the behavior of amplifier concerning input power. The output power versus input available power graph highlighted the output characteristics of the amplifier, showcasing the point at which gain compression begins and quantifying P1dB at 33.658 dBm.

CE 3.16 Transitioning from the ideal lumped components to real components from the CREE PDK was an important step in refining the preliminary design. Replacing smaller inductors with components like low characteristic impedance transmission lines and applying spiral inductors for larger inductors were strategic choices to optimize space utilization. I replaced the ideal capacitors with MIM capacitors, while TFRs substituted resistors as they offered nearly linear and frequency independent resistance. However, the transition from ideal to real components required a recalibration of capacitances and inductances in the matching networks. This adjustment accounted for the introduction of extra losses, which while potentially reducing gain and output power, improved stability and reduced reflection losses.

CE 3.17 I adjusted the real component values for practical feasibility in an actual MMIC layout, considering factors like space occupation and component availability. I added TEEs and CROSSes and applied CURVEs and BENDs for the longer transmission lines, improving the MMIC area efficiency. In the final stage, I generated the layout directly from the schematic, showcasing the transition to real components in the input, inter stage and output matching networks. The result of this process was the full amplifier layout. The 5.2 mm x 1.4 mm dimensions and the total area of 7.28 mm^2 directly influenced the cost of the chip and practical feasibility, validating the successful translation of the design from ideal components to real world MMIC layout.

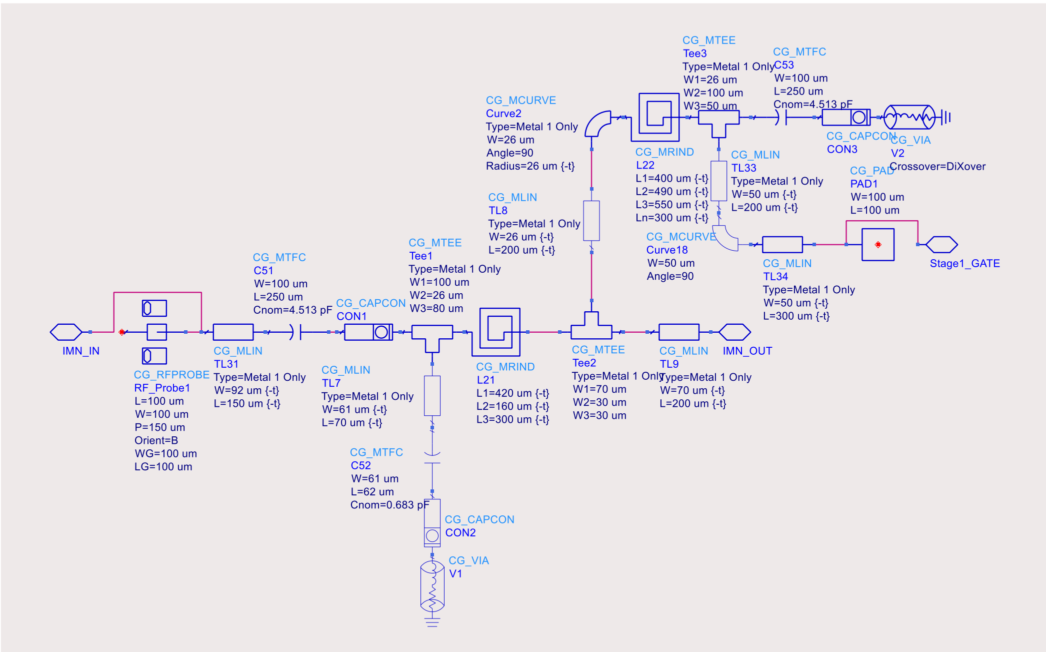


Figure 12: Schematic of Input matching network using real components

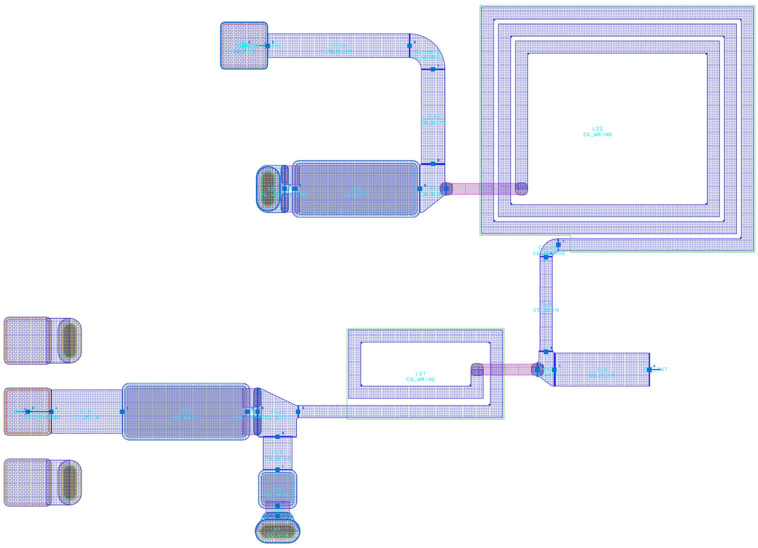


Figure 13: Layout of Input matching network

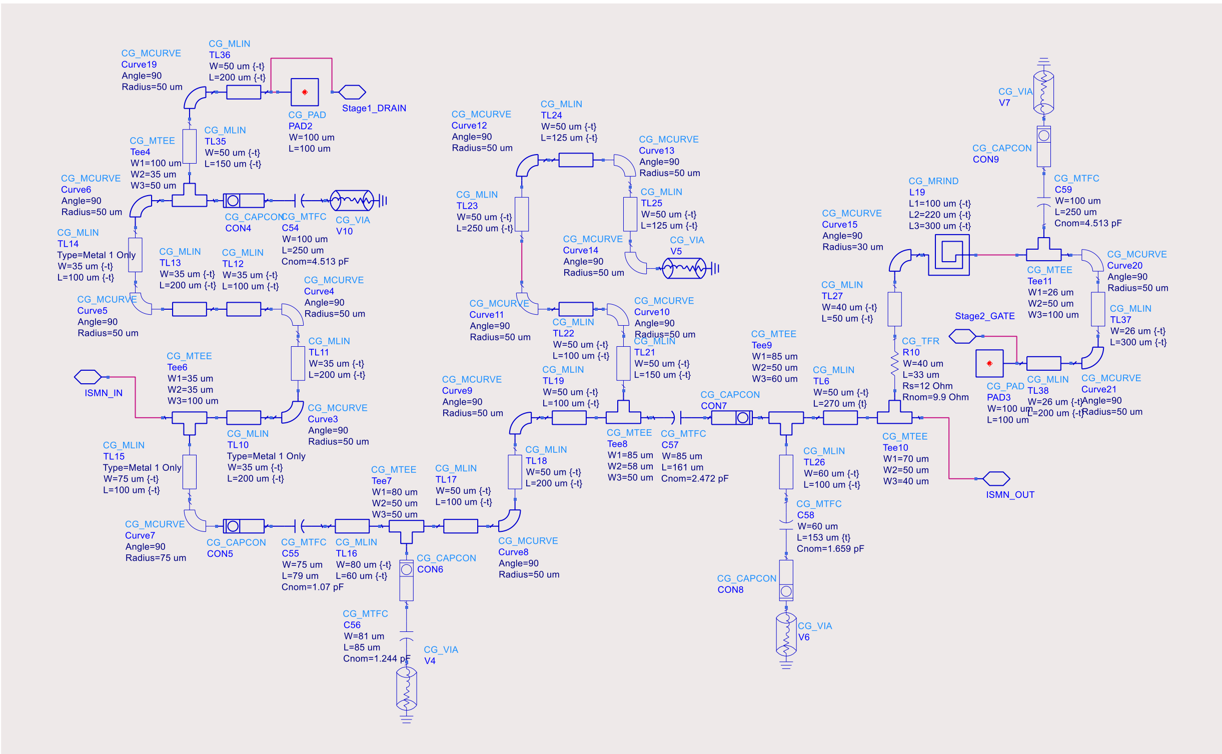


Figure 14: Inter-stage matching network schematic using real components

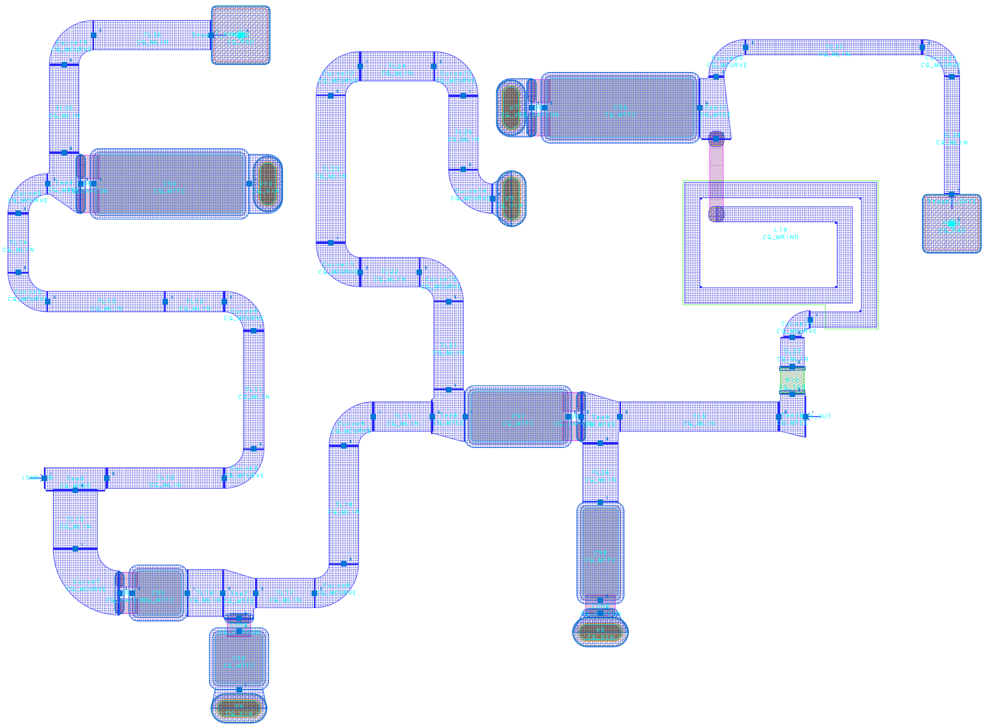


Figure 15: Inter-stage matching network layout

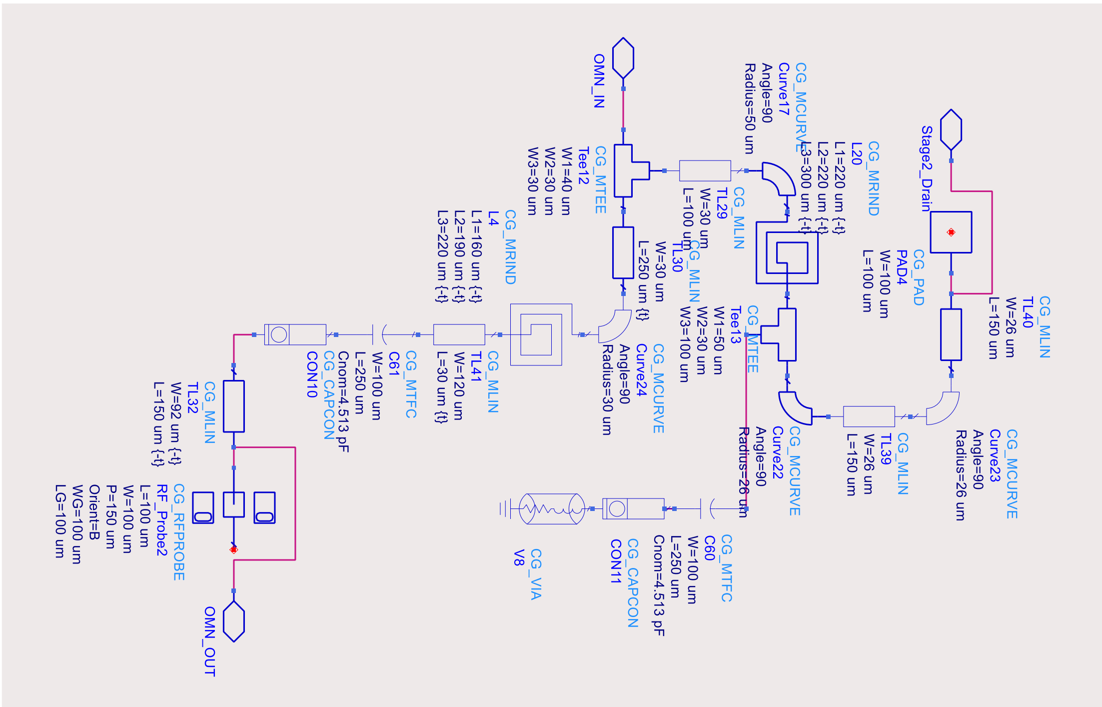


Figure 16: Output matching network using real components

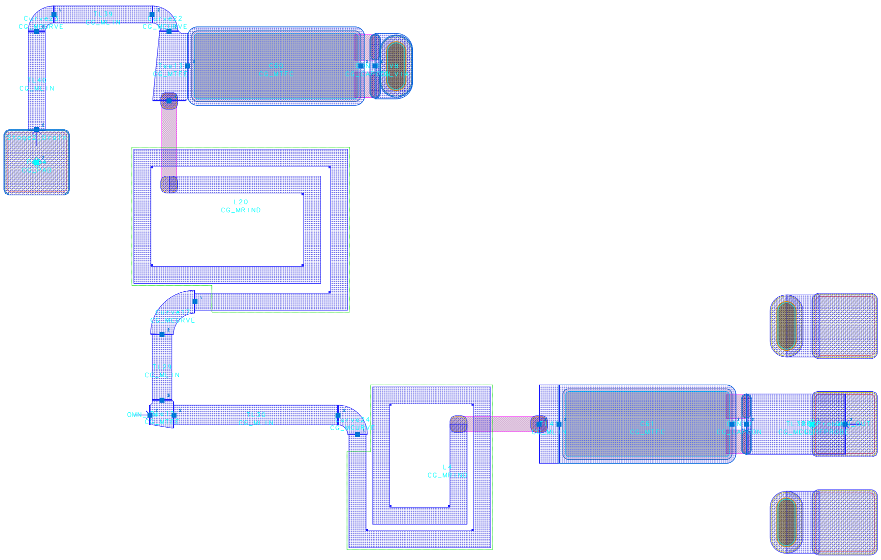


Figure 17: Output matching network layout

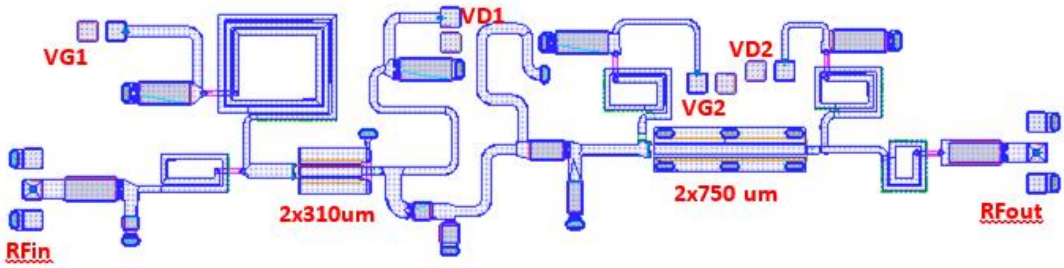


Figure 18: Full amplifier layout

CE 3.18 Throughout this process, I performed simulations, both schematic and EM based layout to verify the real-world performance of the design. The transition from ideal to real components was important, as it better reflected the actual behavior of the circuit. The layout EM simulations were also important for high frequency circuits, as they considered the positions and coupling effects between components, providing a more accurate representation of the response of the circuit. Using a specific substrate for EM simulations, I ensured accurate analysis of passive components.

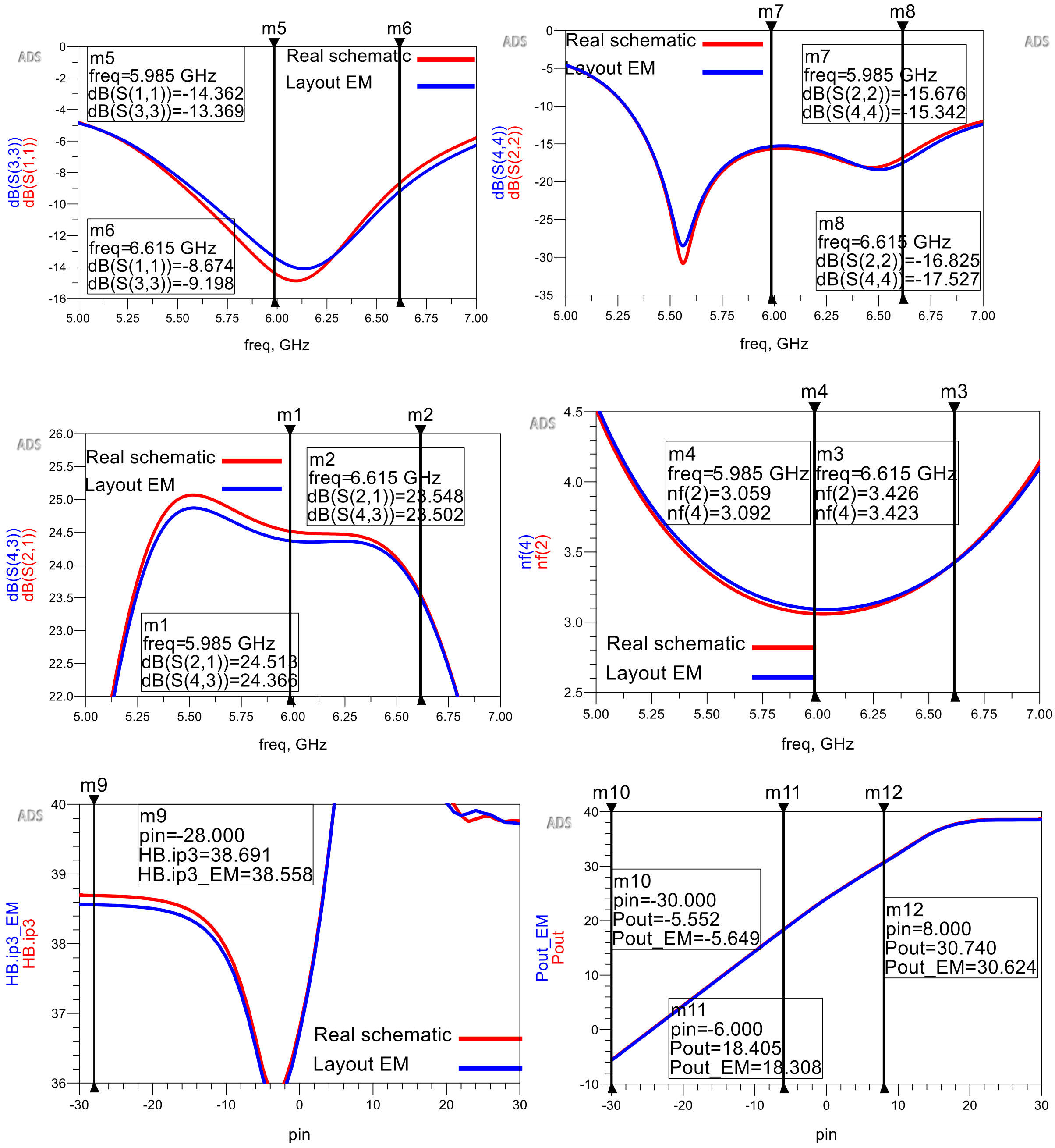


Figure 19: Comparison of layout EM and Schematic

Specification	Requirement	EM simulation	Remarks
Frequency range	5.985 GHz – 6.615 GHz	-	-
Stability	Unconditional stability	Mu > 1 for full frequency range	Satisfied
IRL	< -7 dB	< -8.674 dB	Satisfied
ORL	< -15 dB	< -15.676 dB	Satisfied
Small signal gain	> 21 +-0.5 dB	~23.9 dB +- 0.5 dB	Satisfied
Noise Figure	< 3.5 dB	< 3.423 dB	Satisfied
Output Power	1W	> 1W	Satisfied
P1dB (Input)	> 8 dBm	-6 dBm	Not satisfied
IP3	> 4W	~7.17 W	Satisfied

Table 1: Comparison

CE 3.19 To match the layout simulations and schematic, I generated an .snp file for comparison between the two. The comparison revealed an impressive alignment with most requirements being met exceptionally well. However, there was a deviation that I noted in the P1dB requirements when transitioning from ideal to real components which highlighted the reliability and necessity of real components simulations. Despite this discrepancy, the design achieved nearly perfect specifications. To further improve the reliability and verify the results, I performed layout EM simulations to check if they had a different response. My EM simulations differed slightly from my schematic simulations which showed that the layout was well-designed. I also performed the DRCs to validate the compatibility of the design with the CREE foundry limitations, ensuring fabrication without technological constraints.

SUMMARY

CE 3.20 I designed a low noise and high IP3 amplifier MMIC. I used ADS software to conceptualize the topology and refine the design with ideal components before transitioning to real components from CREE PDK. I made adjustments and simulations to ensure that most specifications were met well, although a shift to real components revealed deviations in P1dB requirements. Despite this, the design met with the expectations marking its success and readiness for fabrication in technological limitations.